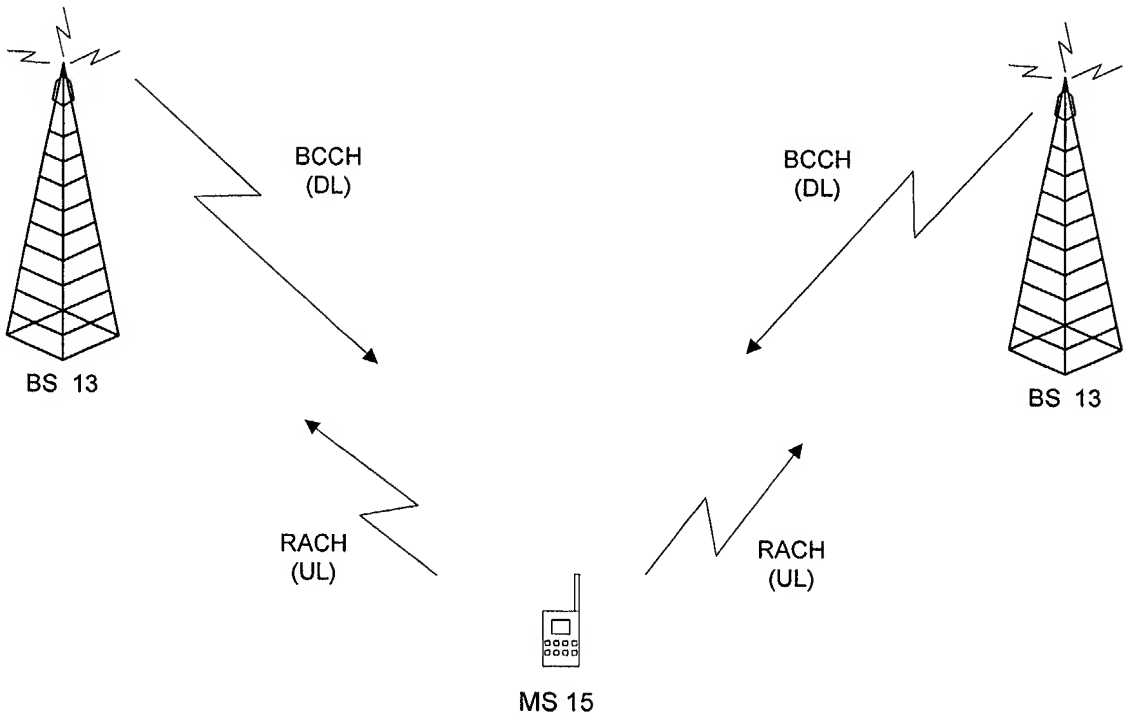


FIG. 1

BPCCH Channel Format

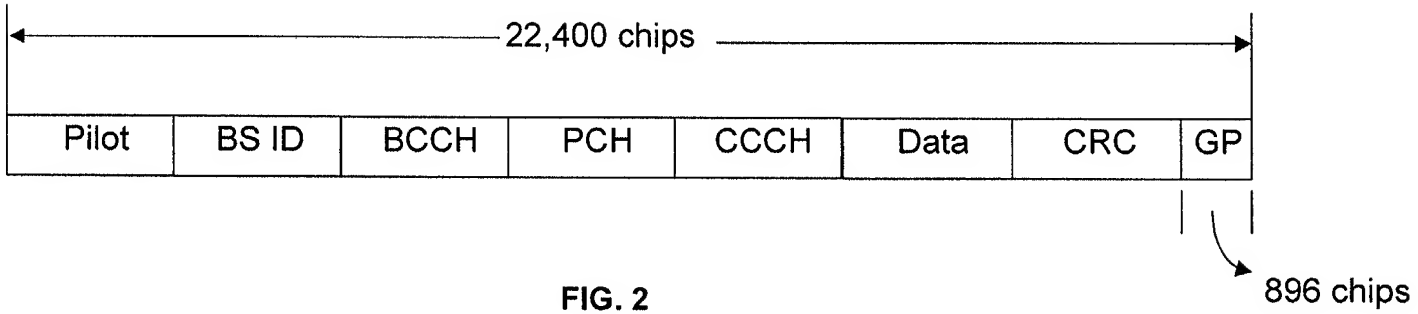


FIG. 2

Random Access Signal Format

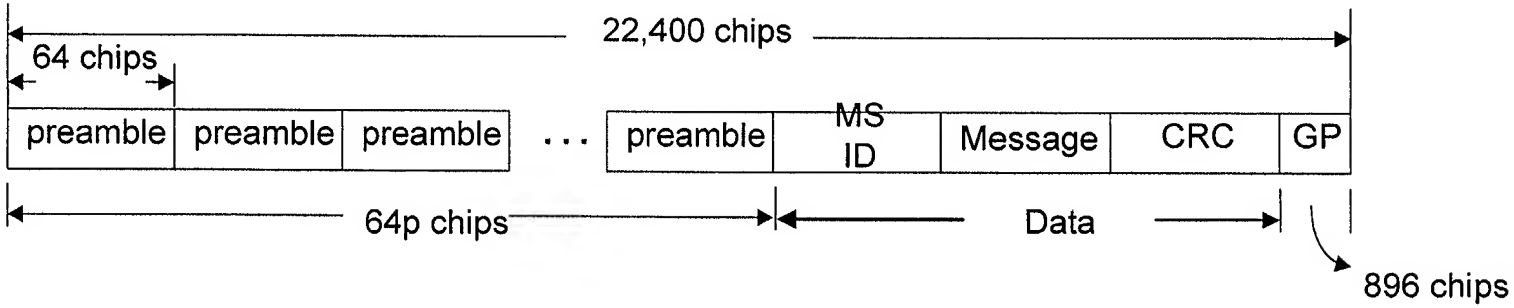


FIG. 4

DRAWING SUBMITTED

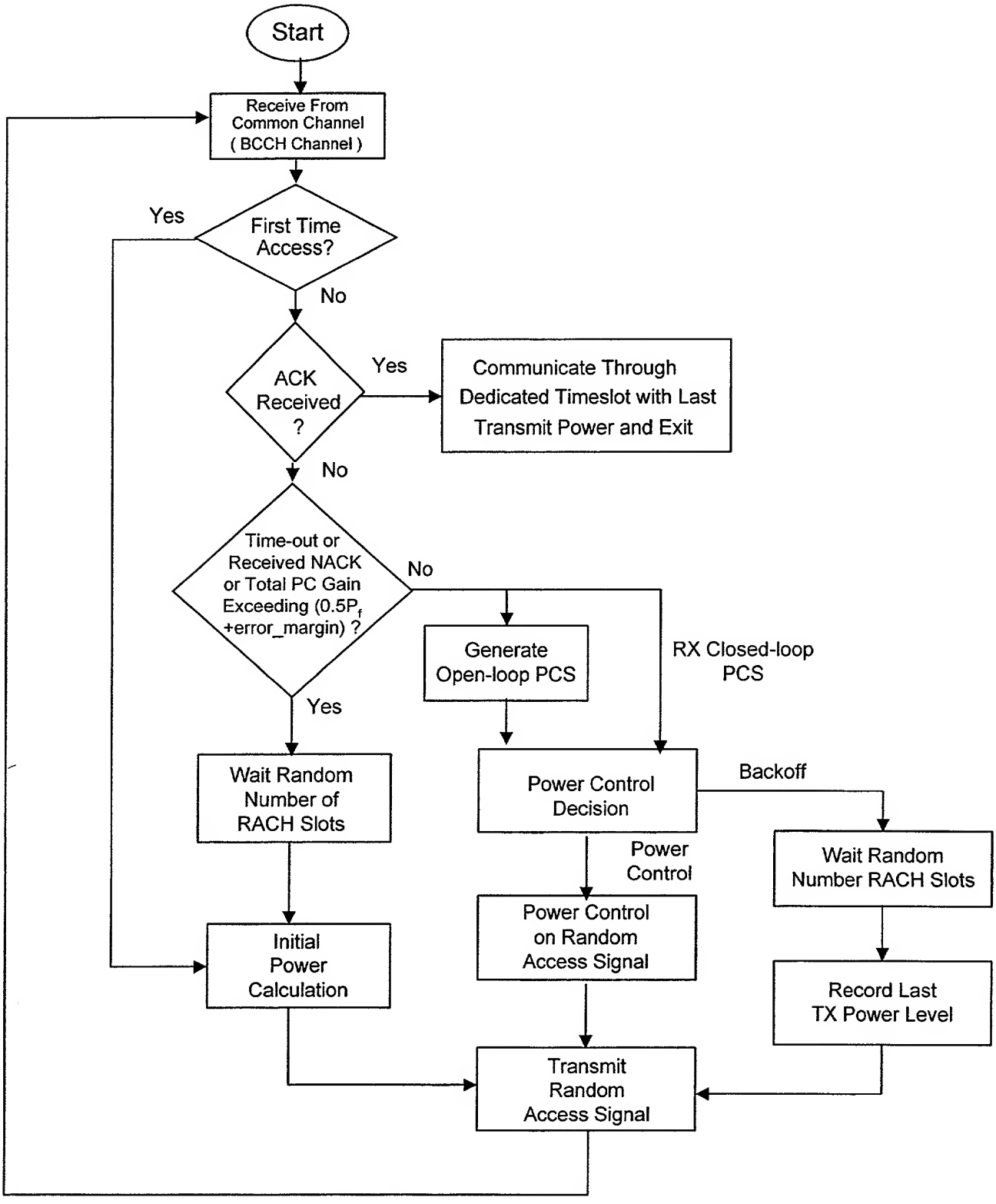


FIG. 3

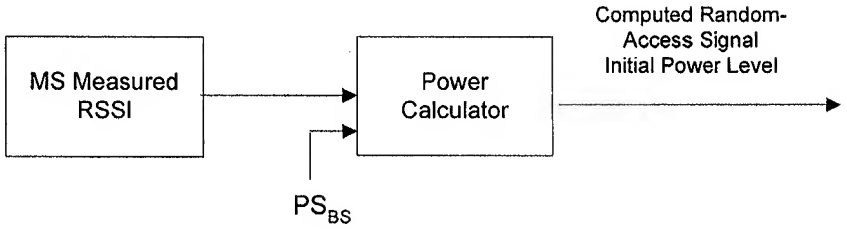


FIG. 5

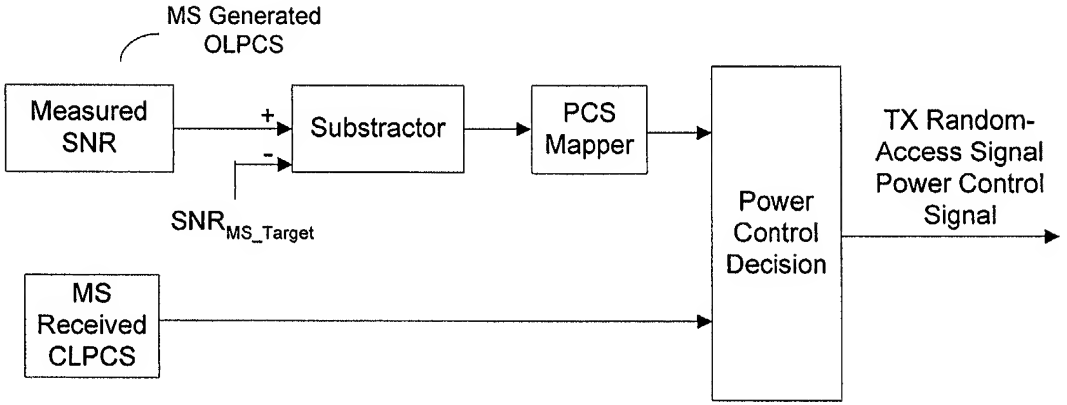


FIG. 6

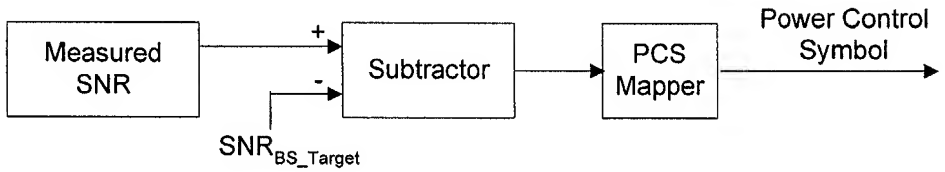


FIG. 7

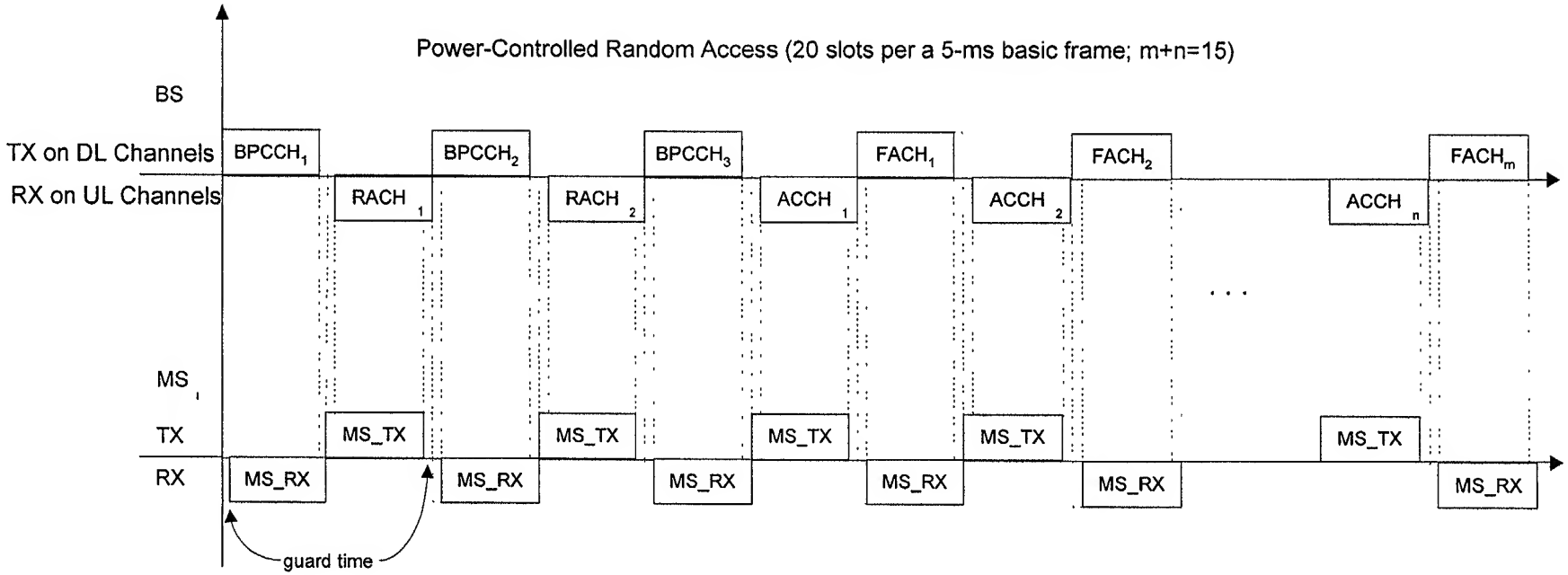

Power-Controlled Random Access (20 slots per a 5-ms basic frame; m+n=15)
BS
TX on DL Channels
RX on UL Channels
MS
TX
RX
BPCCH1
BPCCH2
BPCCH3
FACH1
FACH2
FACHm
RACH 1
RACH 2
ACCH 1
ACCH 2
ACCH n
MS_TX
MS_RX
guard time

FIG. 8

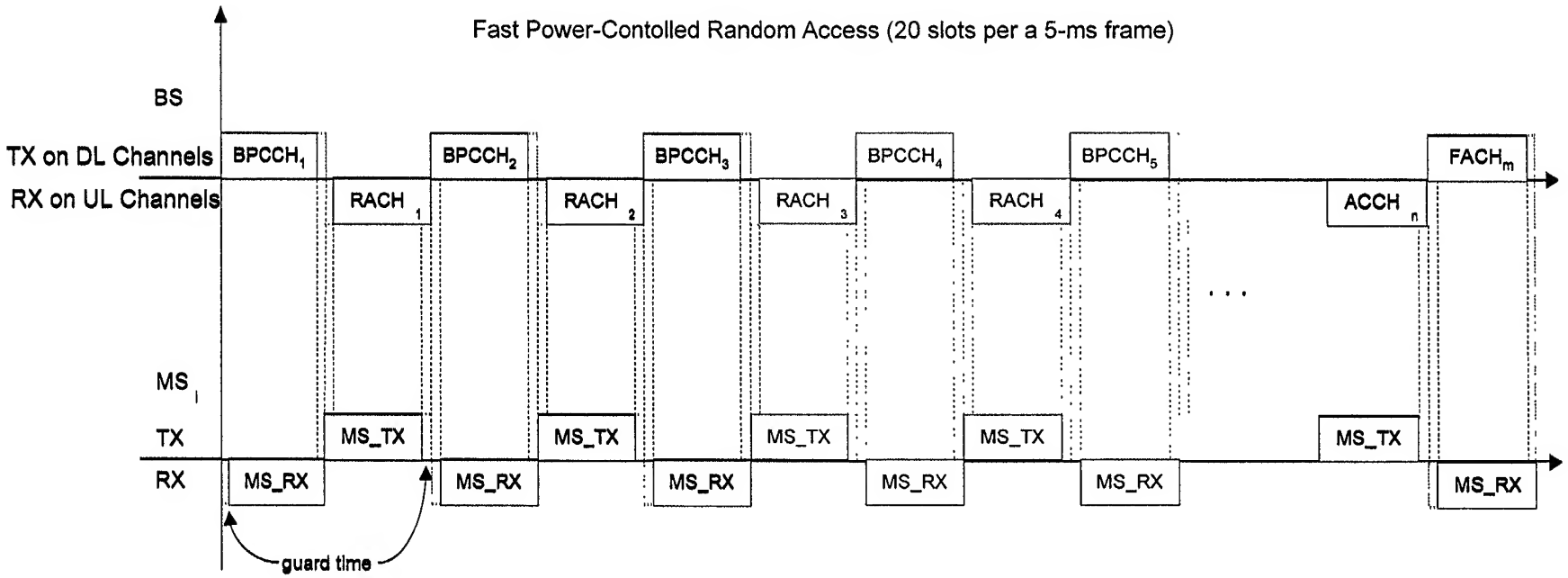

Fast Power-Contolled Random Access (20 slots per a 5-ms frame)
BS
TX on DL Channels
RX on UL Channels
BPCCH1
BPCCH2
BPCCH3
BPCCH4
BPCCH5
FACHm
RACH 1
RACH 2
RACH 3
RACH 4
ACCH n
MS i
TX
RX
MS_TX
MS_RX
guard time

FIG. 9

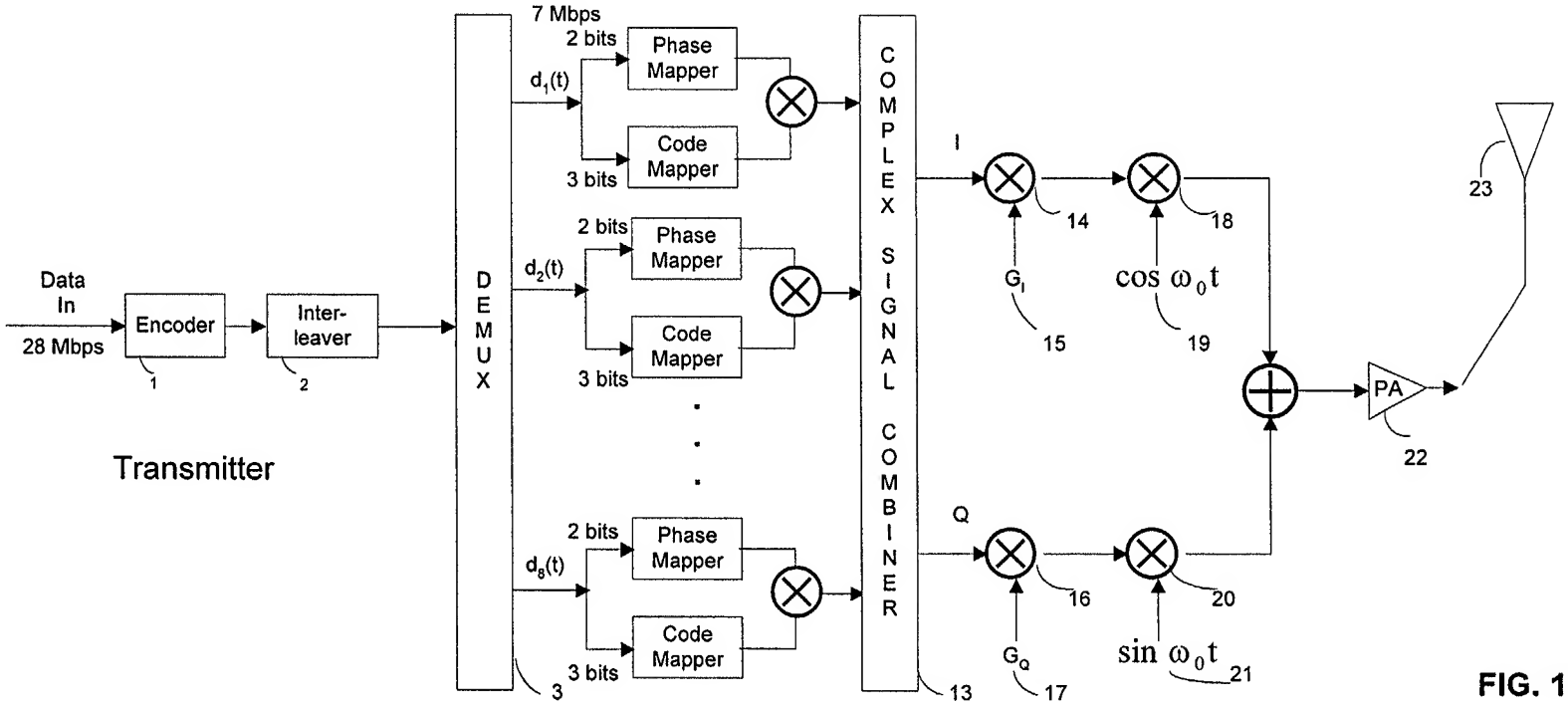
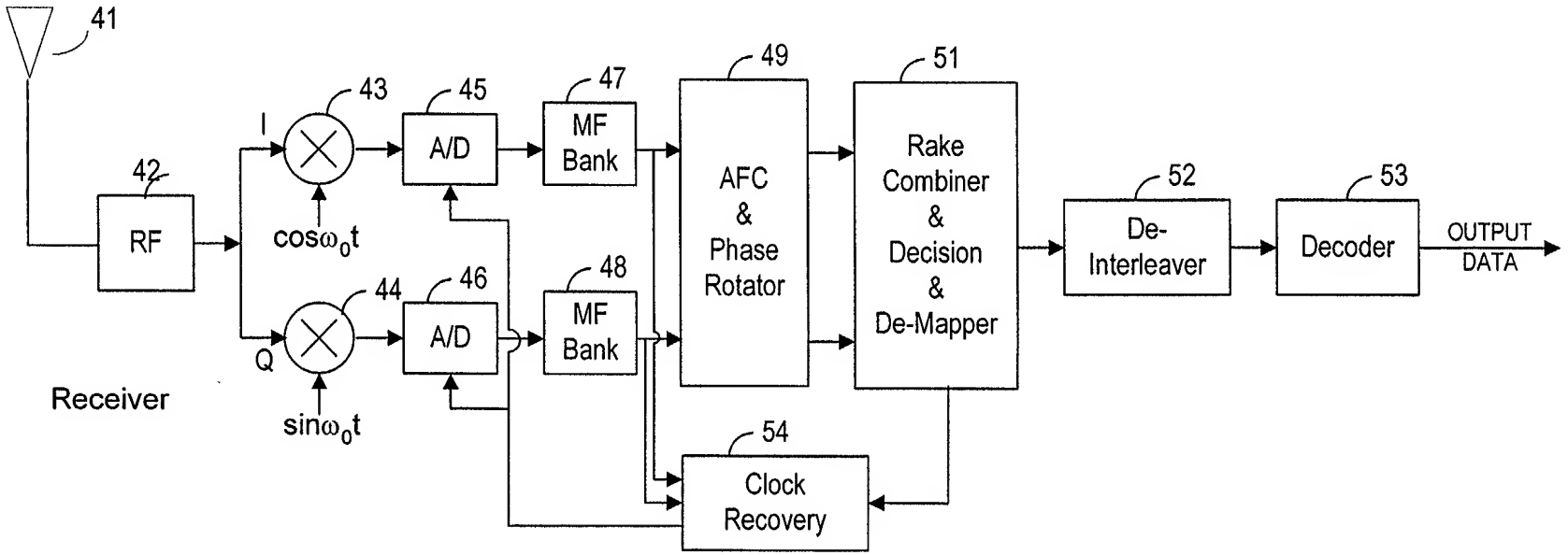

Data In
28 Mbps
Encoder
1
Inter-leaver
2
Transmitter
DEMUX
3
7 Mbps
2 bits
3 bits
$d_1(t)$
$d_2(t)$
$d_8(t)$
Phase Mapper
Code Mapper
COMPLEX SIGNAL COMBINER
13
I
Q
14
15
16
17
18
19
20
21
G_I
G_Q
$\cos \omega_0 t$
$\sin \omega_0 t$
PA
22
23

FIG. 10


41
42
RF
43
44
45
46
47
48
49
51
52
53
I
Q
$\cos\omega_0 t$
$\sin\omega_0 t$
A/D
MF Bank
AFC & Phase Rotator
Rake Combiner & Decision & De-Mapper
De-Interleaver
Decoder
OUTPUT DATA
Receiver
54
Clock Recovery